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09/718,008	11/21/2000	Kenneth Perlin	KPER-4	9323

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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/718,008	PERLIN, KENNETH	
	Examiner	Art Unit	
	Jin-Cheng Wang	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's submission filed on 9/11/2006 has been entered. Claims 1-12 are pending in the application.

Response to Arguments

Applicant's arguments filed September 11, 2006 have been fully considered but are not found persuasive in view of the ground(s) of rejection based on Ebert, D. et al., July 1998, "Texturing and Modeling; A Procedural Approach", Second Edition. AP Professional, Cambridge, pp. 209-274 (hereinafter Ebert et al.).

Ebert et al. including Perlin, the inventor, has disclosed an improved Perlin Noise (as opposed to the OLD Perlin Noise) set forth in applicant's specification. The cited reference discloses a method for creating an appearance of texture in a computer image (see e.g., figures 11-14) comprising the steps of:

Inputting a point $\{ x_d\}$ in D-dimensional geometric space R^3 described via D M bit quantities i_d and D N bit quantities u_d, where id are M bit representations of greatest integers not $> x_d$, and u_d are N bit representations of remainders $(x_d - i_d)$, where M and N are integers > 3 and D = 3, in a computer (*Page 213-218 of the cited reference discloses a point [x, y, z] corresponding to* $\{ x_d \}$, *a point [I, j, k] corresponding to quantities* i_d *and [u, v, w] corresponding to the quantities* u_d);

Computing a pseudo-random hash value at each vertex of a unit cube C surrounding the point (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single*

n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216);

Computing a contribution from each vertex using the hash-value (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216*);

Combining with the computer the contribution from each vertex into a single interpolated result so that each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216. Because the*

algorithm as disclosed in Page 214-218 includes the 3-dimensional evaluation of one x, y, z triplet, it is readily concluded that the execution speed for the same evaluations of the prior art versus what is claimed require the same CPU time on a computer having the same CPU speed. Moreover, the C-codes disclosed in Pages 214-218 include each 3 dimensional evaluation of one x, y, z triplet. When each 3 dimensional evaluation of one x, y, z triplet for the prior art is exactly the same as each 3 dimensional evaluation of one x, y, z triplet as claimed, the CPU time for each such evaluation by the prior art is equal to the CPU time for each evaluation as claimed. It is noted that the C implementation is very efficient, each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ, for example, the C code implemented on the Intel optimizing compiler running on a Pentium 2 or 3 computer).

In Page 7 of Remarks filed 9/11/2006, applicant refers to Page 7, lines 23-27 of the originally filed application to show the subject matter of "inputting a point { x_d } in D-dimensional geometric space R^3 described via D M bit quantities i_d and D N bit quantities u_d, wherein i_d are M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$), where M and N are integers ≥ 4 and D = 3, in a computer". However, the summary at lines 23-27 of Page 7 is flawed for the reasons given below and the claimed subject matter, although differs from, is based on the passage in the summary which describes "inputting a point { x_d } in D-dimensional geometric space R^D described via D M bit quantities i_d and D N bit quantities u_d, wherein i_d are M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$), where M and N are integers ≥ 4, in a computer". The specification however failed to describe the subject matter. For example, "u_d are N bit

representations of remainders ($x_d - i_d$)" failed to establish the relationship between u_d, x_d and i_d. In contrast to the claim language, the specification on Page 13, lines 15-20 discloses "u, v, w signify the fractional position of X, Y, Z above i, j, k, to eight bit precision." Applicant's claim limitation set forth a subtraction operator "-" between x_d and i_d while this subtraction operator failed to describe **the fractional position** of X, Y, Z above i, j, k. According to applicant's specification of Page 13, u_d are not "N bit representations of remainders ($x_d - i_d$)" as claimed. In fact, u_d are the fractional positions of the remainders of the corresponding components of x_d above the corresponding components of i_d, respectively, as opposed to the remainders of the corresponding components of x_d above the corresponding components of i_d. See also Page 9, lines 10-30 of applicant's specification. **u_d is not "N bit representations of remainders" of the vector formed by "($x_d - i_d$)".**

Moreover, "i_d are M bit representations of greatest integers not > x_d" as claimed failed to establish the relationship of i_d with x_d. The comparison operator ">" as recited in the claim are performed for each of M bit representations of greatest integers and each component of the vector x_d, respectively.

Applicant also argues that the cited reference is actually the prior art Perlin noise developed by applicant. The previous version of the Perlin noise was disclosed long time ago by K. Perlin in "An Image Synthesizer", Computer Graphics, Vol. 19, No. 3. See applicant's specification at lines 15-20 of Page 1. The improved Perlin Noise set forth in the cited reference discloses the claimed subject matter. Even though K. Perlin is one of the authors of the cited reference, the cited reference is a printed publication in this country that constitutes a 102(b)

reference, which is published more than one year prior to the date of application for patent in the United States.

Applicant argues that various improvements of the claimed invention are listed in regard to Ebert, specifically in regards to the limitation "where one clock cycle has between 200-300 MHz." In contrary to applicant's arguments, applicant claim limitation requires that "so that each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ". The cited reference discloses an algorithm in Page 214-218 including the 3-dimensional evaluation of one x, y, z triplet. Since the cited reference teaches the identical functionality, thus each 3 dimensional evaluation of one x, y, z triplet requires the identical CPU time when such evaluation is implemented on the same computer.

It is readily concluded that the execution speed for the same evaluations of the prior art versus what is claimed require the same CPU time, e.g., on a computer having the same CPU speed. Moreover, the C-codes disclosed in Pages 214-218 include each 3 dimensional evaluation of one x, y, z triplet. When each 3 dimensional evaluation of one x, y, z triplet for the prior art is exactly the same as each 3 dimensional evaluation of one x, y, z triplet as claimed, the CPU time for each such evaluation by the prior art is equal to the CPU time for each evaluation as claimed. Moreover, it is noted that the C implementation of the cited reference is very efficient, each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ, for example, the C code implemented on the Intel optimizing compiler running on a Pentium 2 or 3 computer.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For example, the base claim 1 recites "inputting a point { x_d } in D-dimensional geometric space R^3 described via D M bit quantities i_d and D N bit quantities u_d, wherein i_d are M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$), where M and N are integers ≥ 4 and D = 3, in a computer".

According to applicant's specification, specifically Page 13 of the specification, applicant at best discloses "a point (X, Y, Z) in R^3, described via six eight-bit quantities i, j, k, u, v, w, where i, j, k are the greatest integers not greater than X, Y, Z, respectively, and u, v, w signify the fractional position of X, Y, Z above i, j, k, to eight-bit precision." The disclosure does not describe the claim limitation of "i_d are M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$)". The disclosure compares each component X, Y, Z of { x_d } with each component i, j, k of { i_d }, respectively. The disclosure computes each component u, v, w of { u_d } from each component X, Y, Z of { x_d } and each component i, j, k of { i_d }. The scalar calculations are performed. There is no disclosure involving the vector calculations/comparisons set forth in the claim 1. Moreover, the disclosure does not describe that u, v, w are the scalar components of { u_d }, X, Y, Z are the scalar components of { x_d } and I, j, k

are the scalar components of { i_d }. Finally, applicant's specification has not established that M and N are different integers.

The specification however failed to describe the subject matter. For example, "u_d are N bit representations of remainders ($x_d - i_d$)" failed to establish the relationship between u_d, x_d and i_d. In contrast to the claim language, the specification on Page 13, lines 15-20 discloses "u, v, w signify the fractional position of X, Y, Z above i, j, k, to eight bit precision." Applicant's claim limitation set forth a subtraction operator "-" between x_d and i_d while this subtraction operator failed to describe **the fractional position** of X, Y, Z above i, j, k. According to applicant's specification of Page 13, u_d are not "N bit representations of remainders ($x_d - i_d$)" as claimed. In fact, u_d are the fractional positions of the remainders of the corresponding components of x_d above the corresponding components of i_d, respectively, as opposed to the remainders of the corresponding components of x_d above the corresponding components of i_d. See also Page 9, lines 10-30 of applicant's specification. **u_d is not "N bit representations of remainders" of the vector formed by "($x_d - i_d$)".**

Moreover, "i_d are M bit representations of greatest integers not > x_d" as claimed failed to establish the relationship of i_d with x_d. The comparison operator ">" as recited in the claim are performed for each of M bit representations of greatest integers and each component of the vector x_d, respectively.

Thus, applicant's specification is not sufficient to establish the claim limitation of "wherein i_d are M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$)." Therefore, the metes and bounds of the coverage of at least claim 1 cannot be ascertained.

To comply with the "written description" requirement of 35 U.S.C. 112, first paragraph, an applicant must convey with reasonable clarity to those skilled in the art that, as of the filling date sought, he or she was in possession of the invention. The invention is, for purposes of the "written description" inquiry, whatever is now claimed. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). For purposes of written description, one shows "possession" by descriptive means such as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. Lockwood v. American Airlines, Inc., 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997). Such descriptive means cannot be found in the disclosure for the inventions of the base claim 1.

Claims 2-11 depend upon the claim 1 and are rejected due to their dependency on the claim 1.

The claim 12 is subject to the same rationale of rejection set forth in the claim 1.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For example, the base claim 1 recites "inputting a point { x_d } in D-dimensional geometric space R^3 described via D M bit quantities i_d and D N bit quantities u_d, wherein i_d are

M bit representations of greatest integers not > x_d and u_d are N bit representations of remainders ($x_d - i_d$), where M and N are integers ≥ 4 and D = 3, in a computer".

However, the claim language is not clear as to the quantities { u_d }, and { i_d } are computed. It is not clear whether M and N are the same integers. It cannot be ascertained from the above claim language how { i_d }are compared with { x_d } and how { u_d } are calculated.

Claims 2-11 depend upon the claim 1 and are rejected due to their dependency on the claim 1.

The claim 12 is subject to the same rationale of rejection set forth in the claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ebert, D. et al., July 1998, "Texturing and Modeling; A Procedural Approach", Second Edition. AP Professional, Cambridge, pp. 209-274 (hereinafter Ebert et al.).

2. Re Claims 1 and 12:

Ebert et al. including Perlin, the inventor, has disclosed an improved Perlin Noise set forth in applicant's specification. The cited reference discloses a method for creating an appearance of texture in a computer image (see e.g., figures 11-14) comprising the steps of:

Inputting a point $\{ x_d \}$ in D-dimensional geometric space R^3 described via D M bit quantities i_d and D N bit quantities u_d, where id are M bit representations of greatest integers not $> x_d$, and u_d are N bit representations of remainders $(x_d - i_d)$, where M and N are integers > 3 and D = 3, in a computer (*Page 213-218 of the cited reference discloses a point [x, y, z] corresponding to $\{ x_d \}$, a point [I, j, k] corresponding to quantities i_d and [u, v, w] corresponding to the quantities u_d*);

Computing a pseudo-random hash value at each vertex of a unit cube C surrounding the point (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216*);

Computing a contribution from each vertex using the hash-value (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the*

successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216);

Combining with the computer the contribution from each vertex into a single interpolated result so that each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ (*Page 214-218 of the cited references discloses mapping lattice points [i, j, k] to indices of G, pre-computing a random permutation table P and using this table to fold [i, j, k] into a single n. It also discloses computing the gradients G[P[P[P[I]+j]+k]] wherein the precomputed arrays P and G contain a pseudo-random permutation and pseudo-random unit-length gradient vectors wherein the successive application of P hashes each lattice point to de-correlate the indices into G. The eight linear functions G(x-i, y-j, z-k) are then trilinearly interpolated using the cubic approximation, Page 216. The cited reference discloses an algorithm in Page 214-218 including the 3-dimensional evaluation of one x, y, z triplet. Since the cited reference teaches the identical functionality, thus each 3 dimensional evaluation of one x, y, z triplet requires the identical CPU time when such evaluation is implemented on the same computer. It is readily concluded that the execution speed for the same evaluations of the prior art versus what is claimed require the same CPU time, e.g., on a computer having the same CPU speed. Moreover, the C-codes disclosed in Pages 214-218 include each 3 dimensional evaluation of one x, y, z triplet. When each 3 dimensional evaluation of one x, y, z triplet for the prior art is exactly the same as each 3 dimensional evaluation of one x, y, z triplet as claimed, the CPU time for each such evaluation by the prior art is equal to the CPU time for each evaluation as claimed. Moreover, it is noted that the C implementation of the*

cited reference is very efficient, each 3 dimensional evaluation of one x, y, z triplet requires only one clock cycle, where one clock cycle is between 200-300 MHZ, for example, the C code implemented on the Intel optimizing compiler running on a Pentium 2 or 3 computer).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ebert, D. et al., July 1998, "Texturing and Modeling; A Procedural Approach", Second Edition. AP Professional, Cambridge, pp. 209-274 (hereinafter Ebert et al.) in view of David M. Lewis "Procedural Texture Mapping on FPGAs", ACM 1999, 1-58113-088-0/99/02, page 112-120 (hereinafter Ye).

5. Claims 2-4:

Ebert et al teach combining the contribution from each vertex into a single result using 3 ease-curve s modules (Page 216).

(2) Ebert et al do not teach (a) six "+" modules combined with seven "L" modules; (b) three "+" modules combined with eight "H" modules; (c) the s modules.

(3) Ye however teaches (a) the "+" modules (figure 8); (b) the "L" modules and the "H" modules (figures 7 and 8); (c) the s modules (figures 6 and 10).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the various combinations of "+" modules, the "L" modules, "H" modules and the s modules into the Ebert et al.'s method for creating a noise because Ye suggests implementing "+" modules in figure 8, XOR modules in figure 8 and s modules in figures 6 and 10 and therefore suggesting an obvious modification.

(5) Therefore, it would have been obvious to implement Ebert's method with some specific numbers/combinations of modules so that it would facilitate an efficient implementation of Perlin Noise based 3-D procedural textures.

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 4 except additional claimed limitation of a look-up table. However, Ye further discloses the claimed limitation of a look-up table (Ye page 116) and Ebert et al teach the lookup table (Ebert Page 209-274).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 5 except additional claimed limitation of computing a gradient direction from each hash value. However, Ye and Ebert further disclose the claimed limitation of computing a gradient direction from each hash value (Ye page 116 and Ebert Pages 209-274).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of allowing the inner product to be done using no multiples, only adds and shifts. However, Ye and Ebert further disclose the claimed limitation of allowing the inner

product to be done using no multiples, only adds and shifts (Ye figures 6-10 and Ebert Page 209-274).

Claim 8:

The claim 8 encompasses the same scope of invention as that of claim 7 except additional claimed limitation of choosing the gradients. However, Ye and Ebert further disclose the claimed limitation of choosing the gradients (Ye page 116 and Ebert Page 209-274).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 8 except additional claimed limitation of using 7 linear-interrelation modules L to perform a trilinear interpolation. However, Ye and Ebert further disclose the claimed limitation of using 7 linear-interrelation modules L to perform a trilinear interpolation (Ye pages 115-116 and Ebert Page 209-274).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 9 except additional claimed limitation of computing an ease curve. However, Ye and Ebert further disclose the claimed limitation of computing an ease curve (Ye page 116 and Ebert Page 209-274).

Claim 11:

The claim 11 encompasses the same scope of invention as that of claim 10 except additional claimed limitation of linear interpolations modules. However, Ye and Ebert further disclose the claimed limitation of linear interpolations modules (Ye figure 7 and Ebert Page 209-274).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (571) 272-7665. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw

KEE M. TUNG
SUPERVISORY PATENT EXAMINER